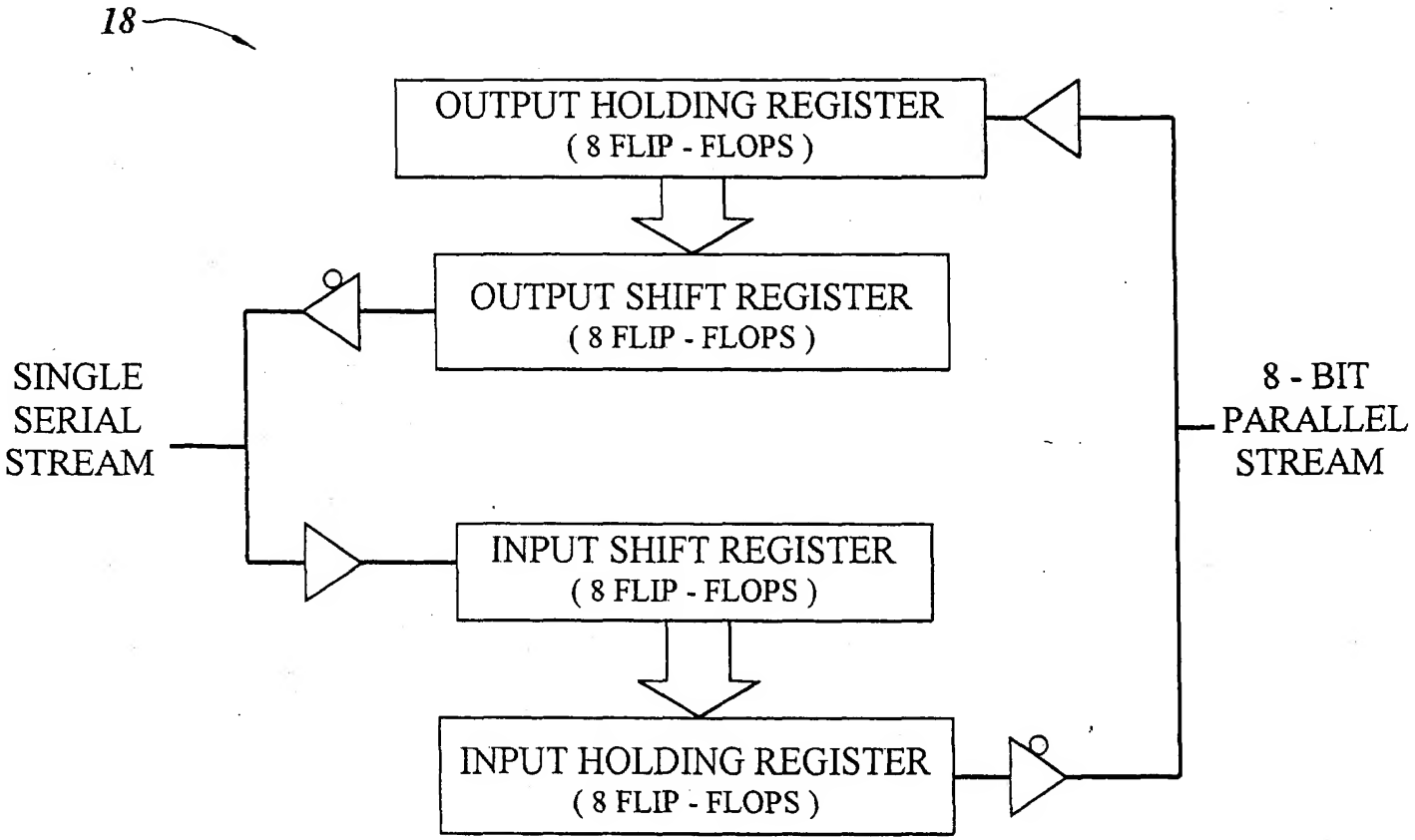

FIG. 1

(PRIOR ART)

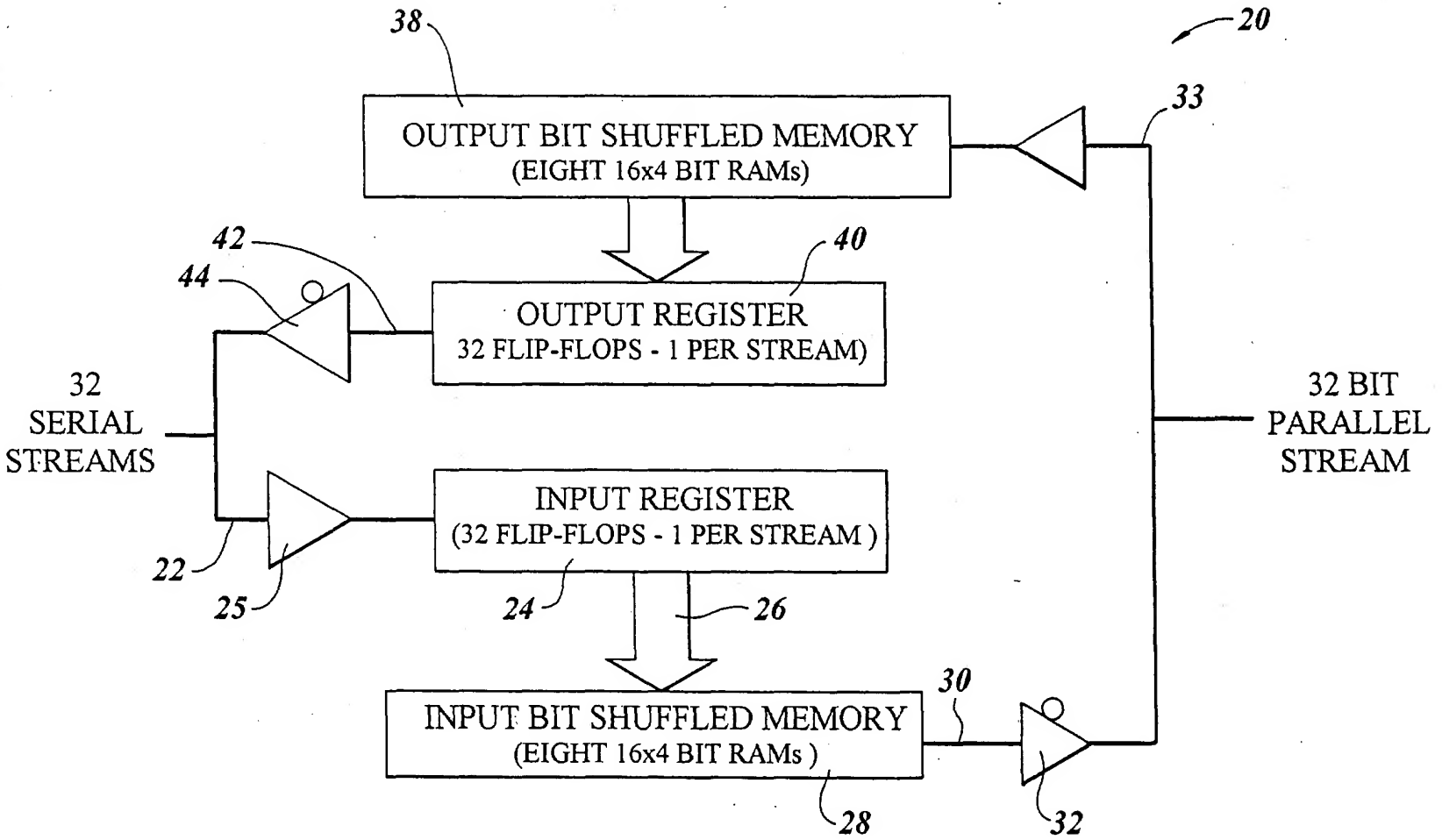
38
20
OUTPUT BIT SHUFFLED MEMORY
(EIGHT 16x4 BIT RAMs)
33
42
40
44
OUTPUT REGISTER
32 FLIP-FLOPS - 1 PER STREAM)
32
SERIAL
STREAMS
32 BIT
PARALLEL
STREAM
INPUT REGISTER
(32 FLIP-FLOPS - 1 PER STREAM)
22
25
24
26
30
INPUT BIT SHUFFLED MEMORY
(EIGHT 16x4 BIT RAMs)
28
32

FIG. 2

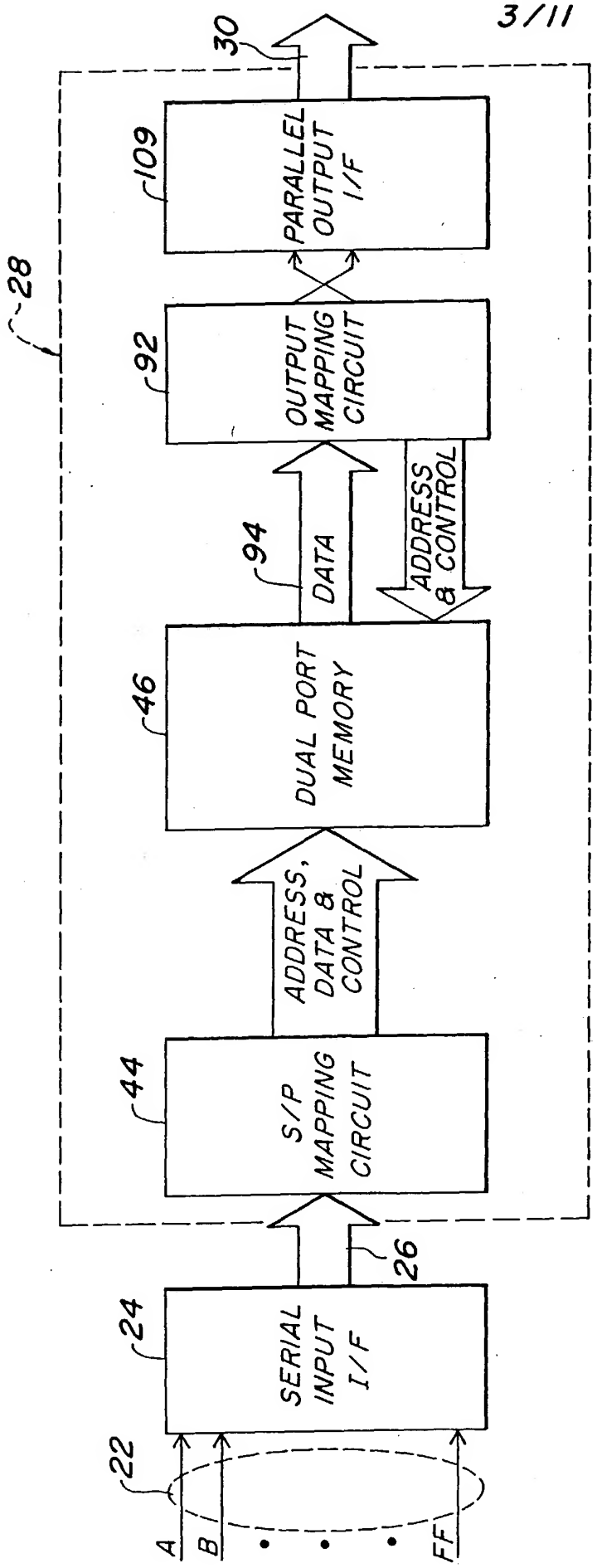
22
A
B
FF
24
SERIAL INPUT I/F
26
44
S/P MAPPING CIRCUIT
ADDRESS, DATA & CONTROL
46
DUAL PORT MEMORY
94
DATA
ADDRESS & CONTROL
92
OUTPUT MAPPING CIRCUIT
109
PARALLEL OUTPUT I/F
30
28

FIG. 3

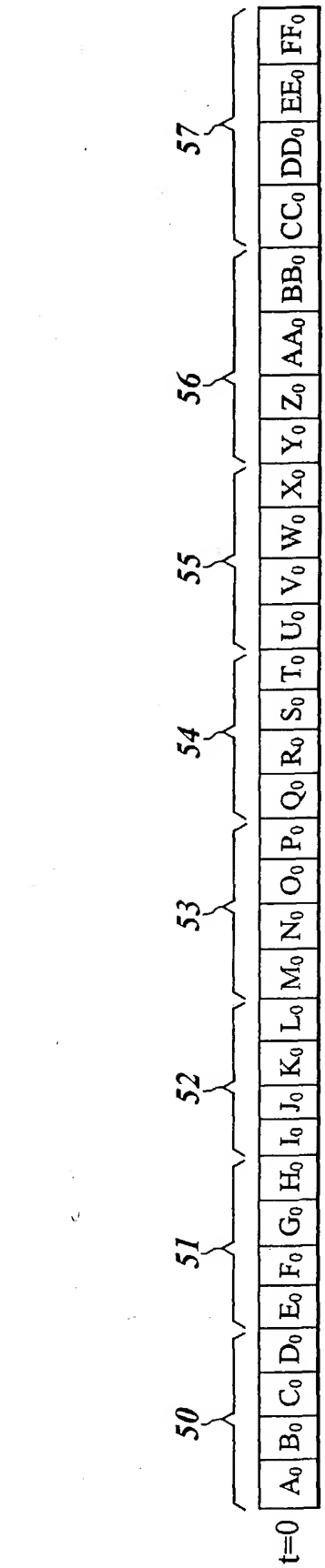
t=0
A0 B0 C0 D0 E0 F0 G0 H0 I0 J0 K0 L0 M0 N0 O0 P0 Q0 R0 S0 T0 U0 V0 W0 X0 Y0 Z0 AA0 BB0 CC0 DD0 EE0 FF0
50
51
52
53
54
55
56
57

FIG. 4A

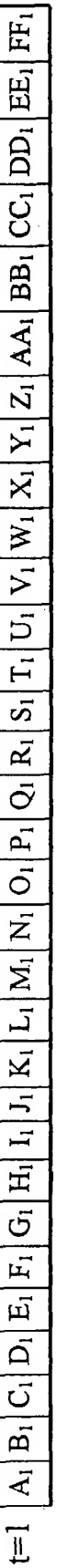
t=1
A1 B1 C1 D1 E1 F1 G1 H1 I1 J1 K1 L1 M1 N1 O1 P1 Q1 R1 S1 T1 U1 V1 W1 X1 Y1 Z1 AA1 BB1 CC1 DD1 EE1 FF1
70
71
72
73
74
75
76
77

FIG. 4B

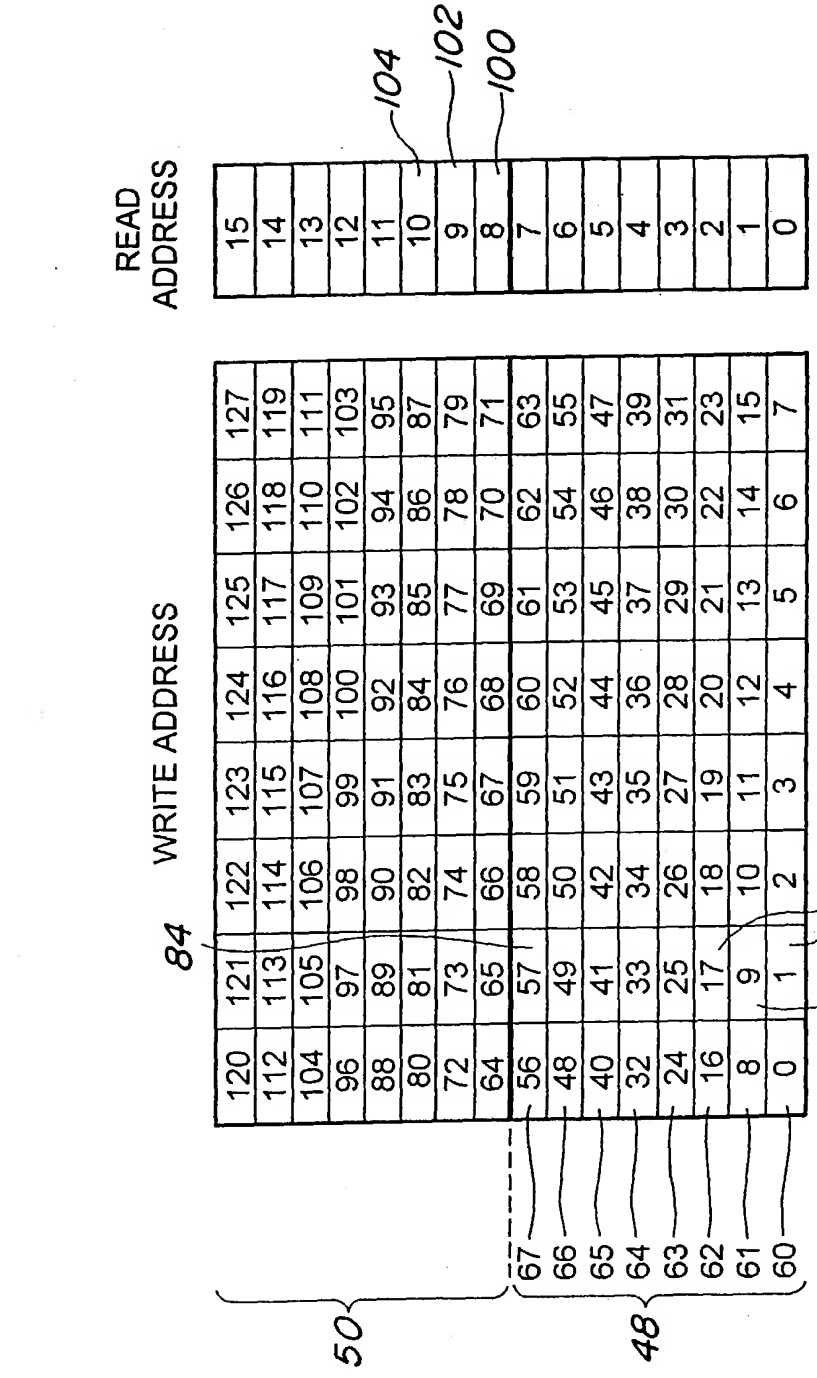
READ ADDRESS
WRITE ADDRESS
84
82
81
80
104
102
100
50
48
67
66
65
64
63
62
61
60

FIG. 5

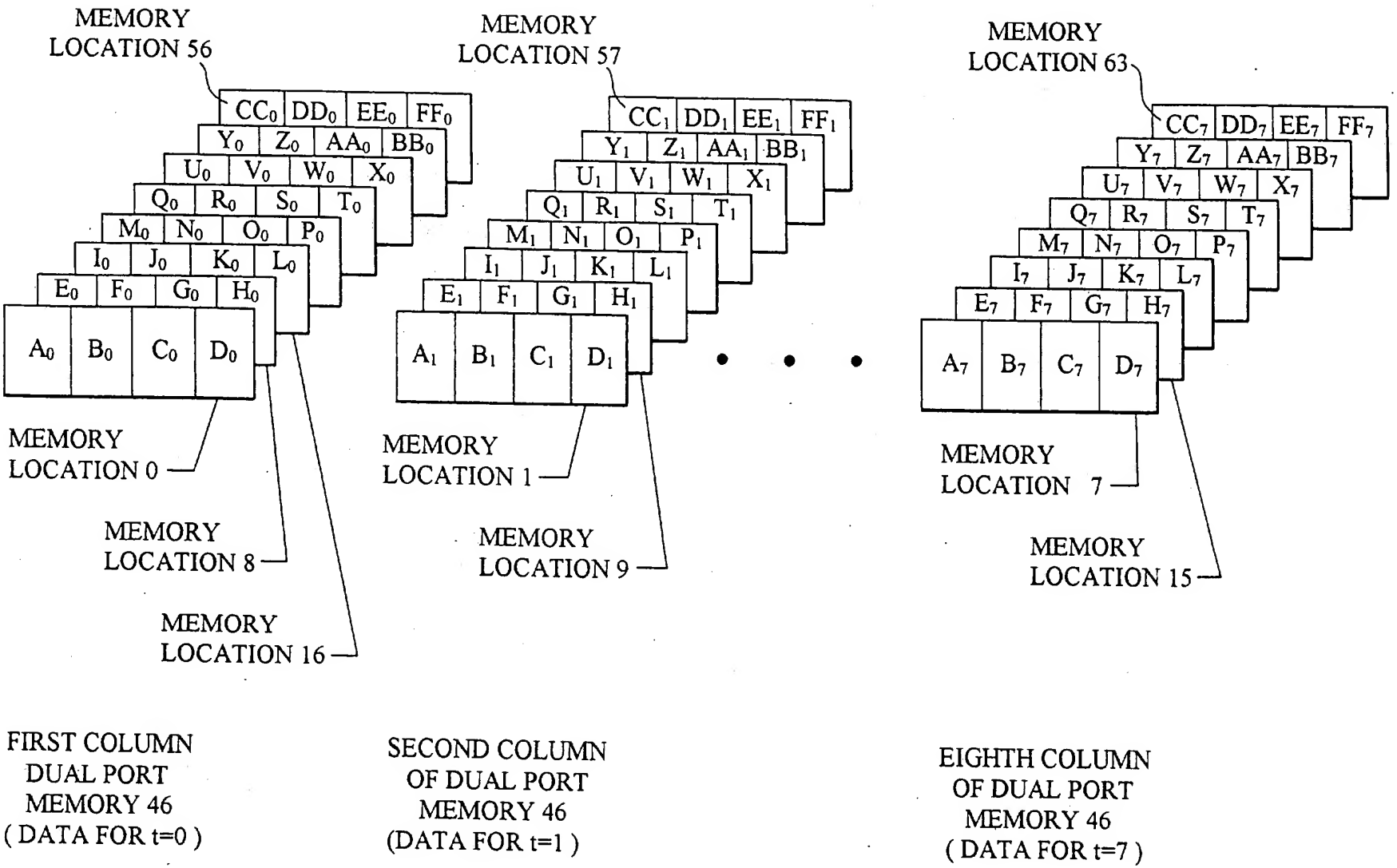
MEMORY LOCATION 56
MEMORY LOCATION 57
MEMORY LOCATION 63
CC0 DD0 EE0 FF0
Y0 Z0 AA0 BB0
U0 V0 W0 X0
Q0 R0 S0 T0
M0 N0 O0 P0
I0 J0 K0 L0
E0 F0 G0 H0
A0 B0 C0 D0
CC1 DD1 EE1 FF1
Y1 Z1 AA1 BB1
U1 V1 W1 X1
Q1 R1 S1 T1
M1 N1 O1 P1
I1 J1 K1 L1
E1 F1 G1 H1
A1 B1 C1 D1
CC7 DD7 EE7 FF7
Y7 Z7 AA7 BB7
U7 V7 W7 X7
Q7 R7 S7 T7
M7 N7 O7 P7
I7 J7 K7 L7
E7 F7 G7 H7
A7 B7 C7 D7
MEMORY LOCATION 0
MEMORY LOCATION 8
MEMORY LOCATION 16
MEMORY LOCATION 1
MEMORY LOCATION 9
MEMORY LOCATION 7
MEMORY LOCATION 15
FIRST COLUMN DUAL PORT MEMORY 46 (DATA FOR t=0)
SECOND COLUMN OF DUAL PORT MEMORY 46 (DATA FOR t=1)
EIGHTH COLUMN OF DUAL PORT MEMORY 46 (DATA FOR t=7)

FIG. 6

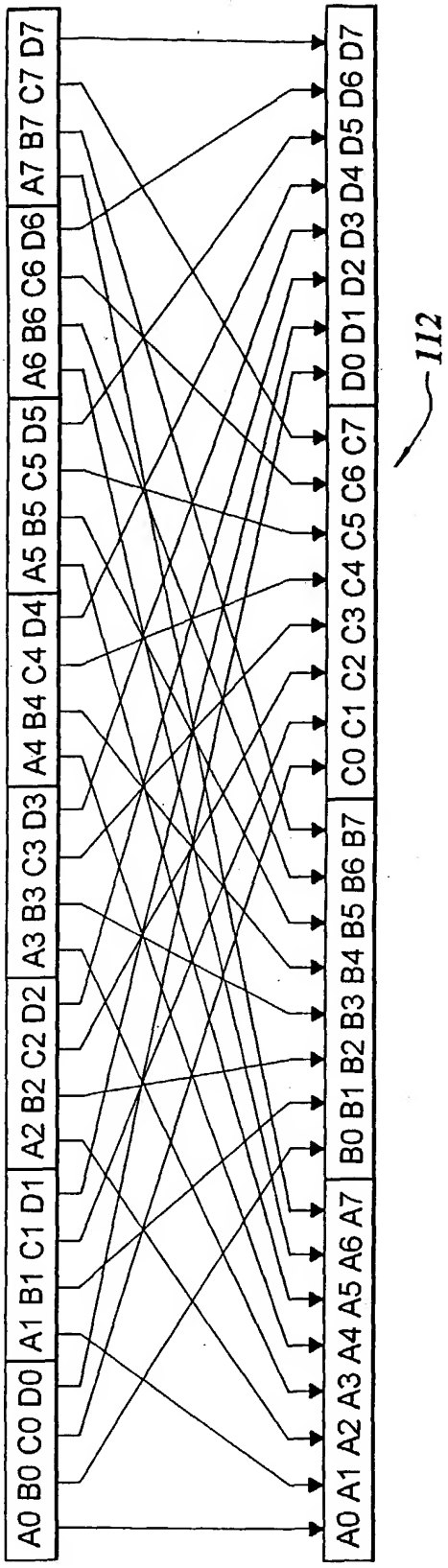
110
A0 B0 C0 D0
A1 B1 C1 D1
A2 B2 C2 D2
A3 B3 C3 D3
A4 B4 C4 D4
A5 B5 C5 D5
A6 B6 C6 D6
A7 B7 C7 D7
112
A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7
C0 C1 C2 C3 C4 C5 C6 C7
D0 D1 D2 D3 D4 D5 D6 D7

FIG. 7

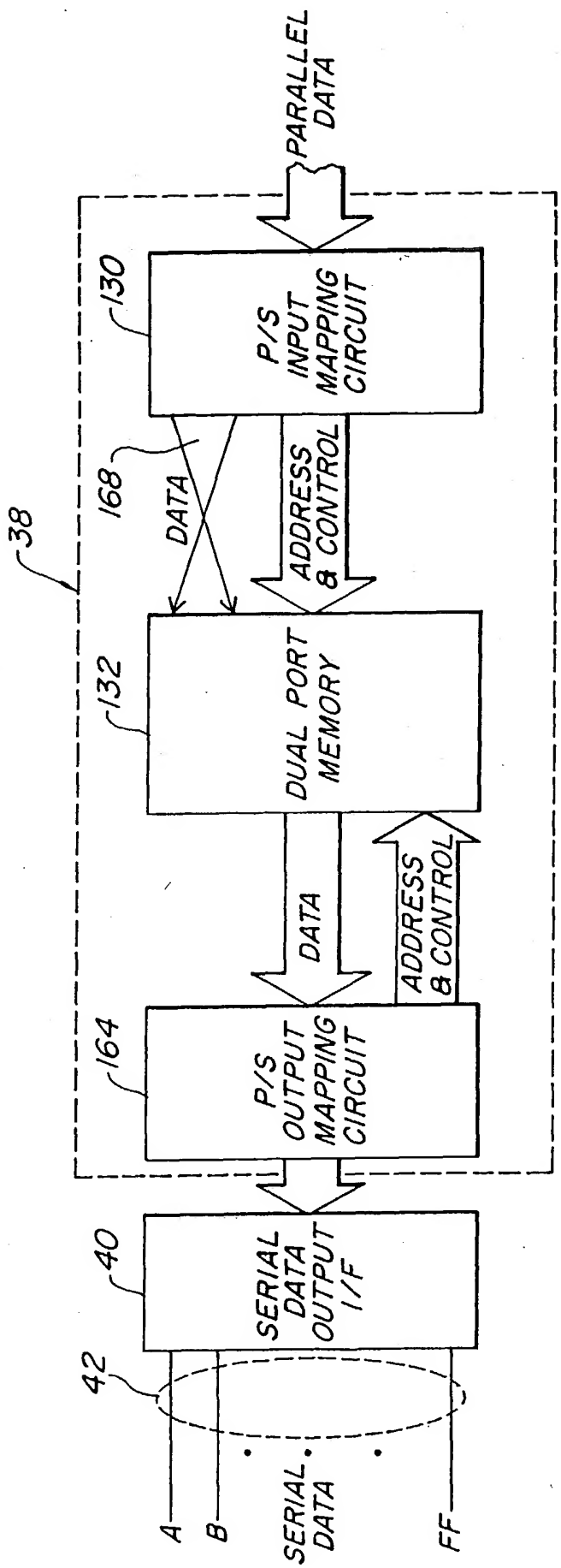
PARALLEL DATA
130
P/S INPUT MAPPING CIRCUIT
168
DATA
ADDRESS & CONTROL
38
132
DUAL PORT MEMORY
DATA
ADDRESS & CONTROL
164
P/S OUTPUT MAPPING CIRCUIT
40
SERIAL DATA OUTPUT I/F
42
A
B
SERIAL DATA
FF

FIG. 8

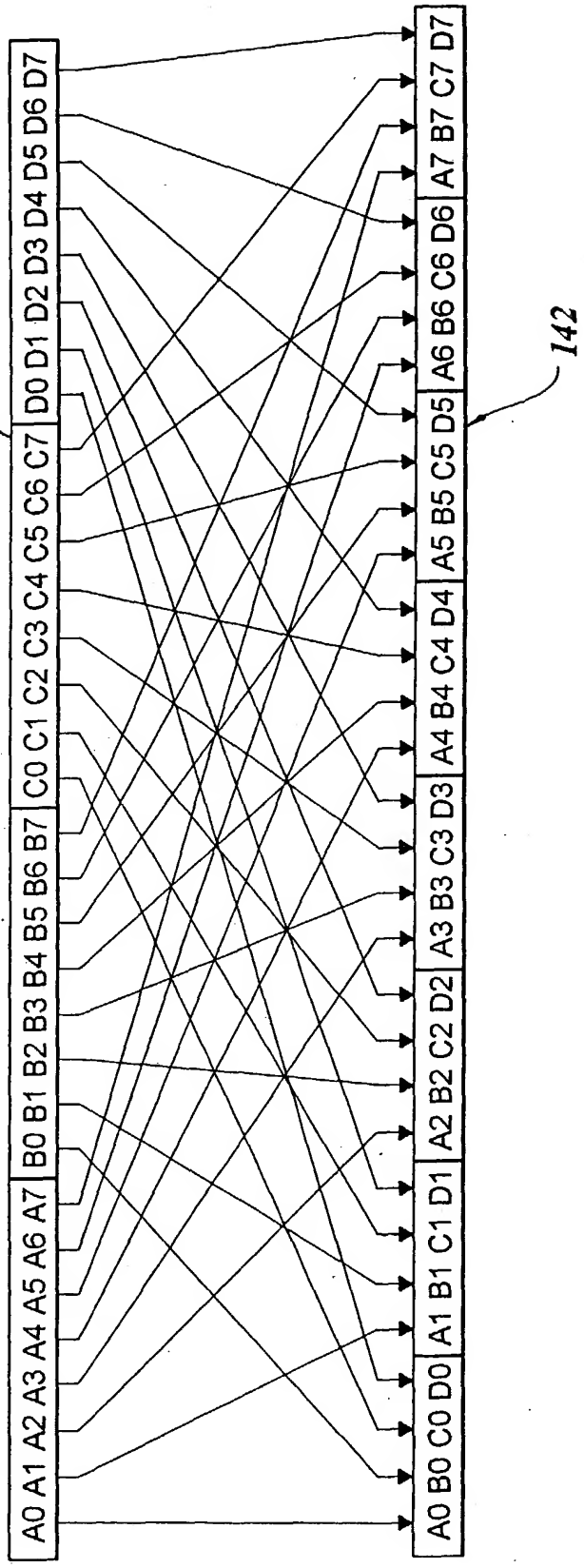
140
142
A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7
C0 C1 C2 C3 C4 C5 C6 C7
D0 D1 D2 D3 D4 D5 D6 D7
A0 B0 C0 D0
A1 B1 C1 D1
A2 B2 C2 D2
A3 B3 C3 D3
A4 B4 C4 D4
A5 B5 C5 D5
A6 B6 C6 D6
A7 B7 C7 D7

FIG. 9

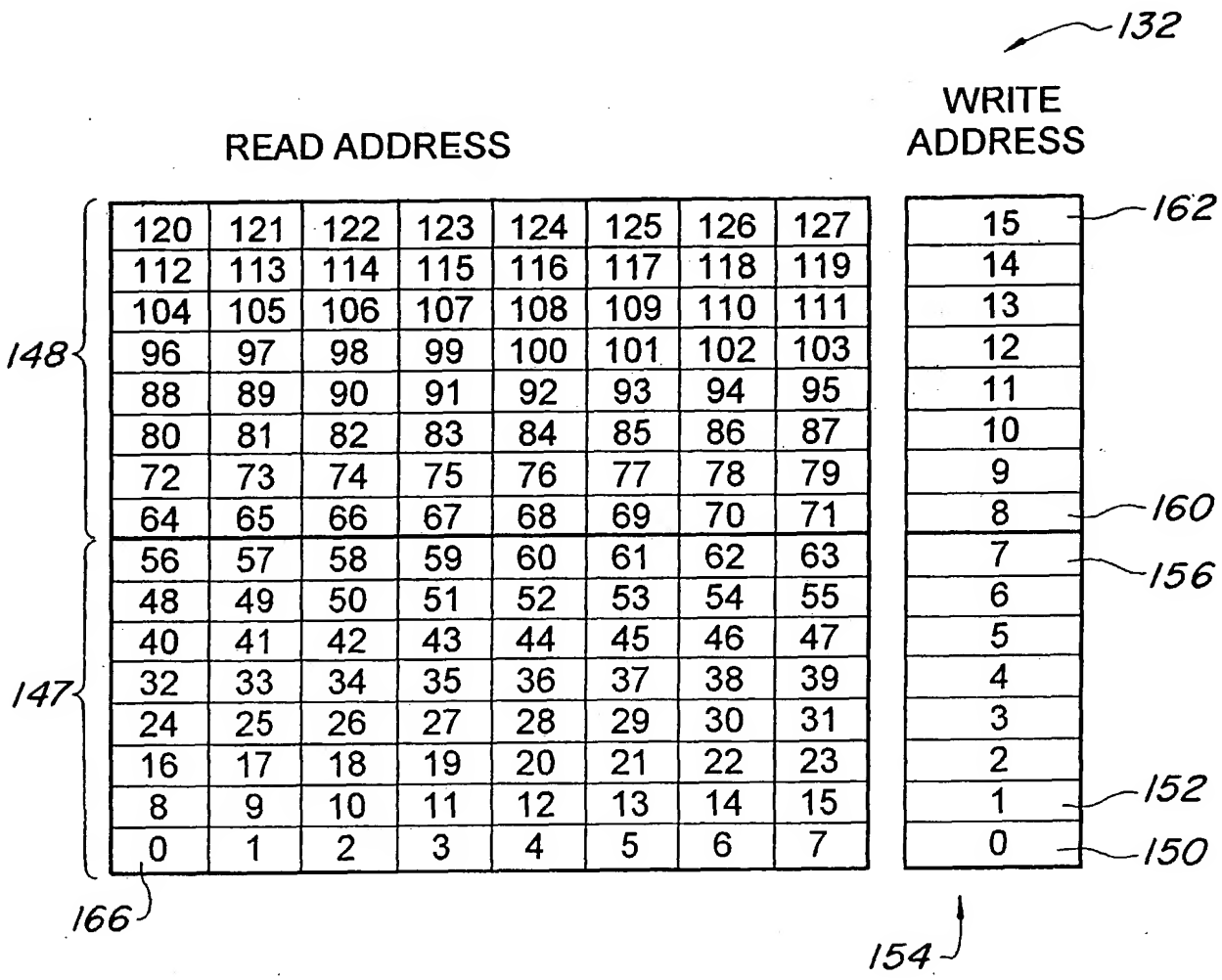
132
READ ADDRESS
WRITE ADDRESS
120 121 122 123 124 125 126 127
112 113 114 115 116 117 118 119
104 105 106 107 108 109 110 111
96 97 98 99 100 101 102 103
88 89 90 91 92 93 94 95
80 81 82 83 84 85 86 87
72 73 74 75 76 77 78 79
64 65 66 67 68 69 70 71
56 57 58 59 60 61 62 63
48 49 50 51 52 53 54 55
40 41 42 43 44 45 46 47
32 33 34 35 36 37 38 39
24 25 26 27 28 29 30 31
16 17 18 19 20 21 22 23
8 9 10 11 12 13 14 15
0 1 2 3 4 5 6 7
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
148
147
166
154
162
160
156
152
150

FIG. 10

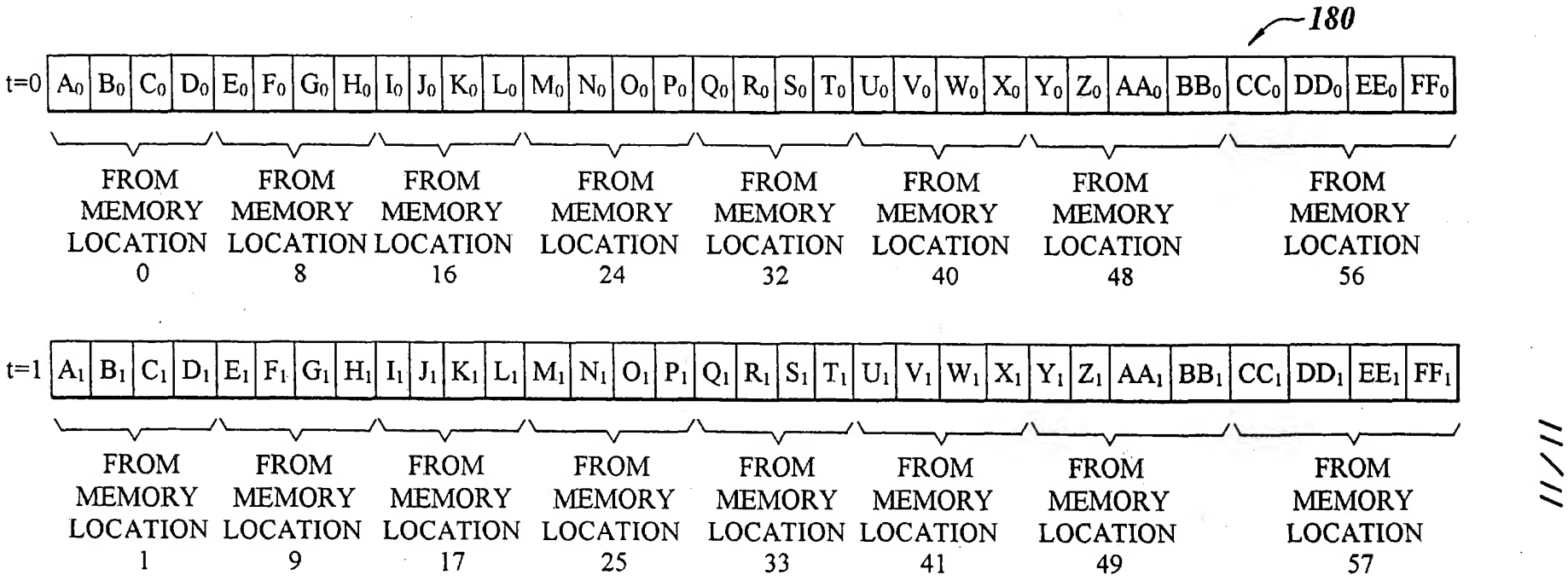
180
t=0
A0 B0 C0 D0 E0 F0 G0 H0 I0 J0 K0 L0 M0 N0 O0 P0 Q0 R0 S0 T0 U0 V0 W0 X0 Y0 Z0 AA0 BB0 CC0 DD0 EE0 FF0
FROM MEMORY LOCATION 0
FROM MEMORY LOCATION 8
FROM MEMORY LOCATION 16
FROM MEMORY LOCATION 24
FROM MEMORY LOCATION 32
FROM MEMORY LOCATION 40
FROM MEMORY LOCATION 48
FROM MEMORY LOCATION 56
t=1
A1 B1 C1 D1 E1 F1 G1 H1 I1 J1 K1 L1 M1 N1 O1 P1 Q1 R1 S1 T1 U1 V1 W1 X1 Y1 Z1 AA1 BB1 CC1 DD1 EE1 FF1
FROM MEMORY LOCATION 1
FROM MEMORY LOCATION 9
FROM MEMORY LOCATION 17
FROM MEMORY LOCATION 25
FROM MEMORY LOCATION 33
FROM MEMORY LOCATION 41
FROM MEMORY LOCATION 49
FROM MEMORY LOCATION 57

FIG. 11